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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/878,401	06/12/2001	Jae Yong Park	2658-0268P	2192
2292	7590	06/22/2005	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			NGUYEN, JENNIFER T	
			ART UNIT	PAPER NUMBER
			2674	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/878,401	PARK, JAE YONG
	Examiner	Art Unit
	Jennifer T. Nguyen	2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 12 June 2001.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-11 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-11 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____

DETAILED ACTION

1. This Office action is responsive to Amendment filed on 02/01/2005.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawada et al. (Patent No. US 6,774,872).

Regarding claims 1 and 11, referring to Fig. 4C, Kawada teaches an electro-luminescence display (col. 1, lines 64-67) comprising:

an electro-luminescence panel having a first surface including a display area (15) and an opposite face having a non-display area (11);
driving circuit boards (23) for applying driving signals to a gate line and a data line provided on the opposite face having the non-display are of the electro-luminescence panel; and tape carrier packages (21a') connecting the driving circuit boards (23) and the electro-luminescence panel (11) wherein the tape carrier packages (21a') and the driving circuit boards (23) are disposed upon the non-display area (11) within the panel (from col. 4, line 56 to col. 5, line 10).

Kawada differs from claims 1 and 11 in that he does not specifically teach the tape carrier packages connecting the driving circuit boards and the electro-luminescence panel in a planar state. Kawada teaches the tape carrier packages (21a') connecting the driving circuit boards (23)

mounted upon heat sink block (26) of the electro-luminescence panel (11) (Fig. 4C). However, it would have been obvious to minimize the size of the heat sink block in order to provide a display that is capable of being made having a small thickness.

Regarding claims 2 and 6, Kawada teaches the driving circuit boards include: a gate driving circuit for applying driving signals to the gate lines; and a data driving circuit for applying driving signals to the data lines (inherently in a electro-luminescence panel, col. 1, lines 9-52).

Regarding claims 3-5, Kawada further teaches the driving circuit boards (23) include a plurality of output pads (21b') electrically connected to the tape carrier packages and panel includes a plurality of input pads (between PCB 23 and TAB 21a') that are provided at the non-display area and electrically connected to the tape carrier packages (Fig. 4C, from col. 4, line 56 to col. 5, line 10).

Regarding claim 7, Kawada further teaches the tape carrier packages (21a') has a first side for connecting the driving circuit boards (23) to the panel (11) and a second side for holding a computer chip (IC 21) (Fig. 4C, from col. 4, line 56 to col. 5, line 10).

Regarding claims 8-10, Kawada further teaches a substantial portion of each of said tape carrier packages (21a') having a first portion disposed in a common plane with said driving circuit boards (23) and connected to the panel (11) and a second portion disposed in a contiguous plane to the common plane of said panel and said first portion (from col. 4, line 56 to col. 5, line 10).

Response to Arguments

4. Applicants' arguments filed 02/01/05, have been fully considered but they are not persuasive because as follows:

In response to Applicants' argument filed "in the first place, the Office action presents no objective factual evidence or reasoning to support this speculative conclusion... In the second place, plasma display panels, including that of Kawada, are normally of a relatively small thickness, and there is no objective factual evidence of record presented to show that there is a need to make Kawada's display panel smaller than it is. In the third place, there is no objective factual evidence of record presented to make it smaller by providing a claimed feature that is admittedly missing from Kawada". Examiner respectfully disagrees, although Kawada does not specifically teach the tape carrier packages connecting the driving circuit boards and the electro-luminescence panel in a planar state. He teaches the tape carrier packages (21a') connecting the driving circuit boards (23) mounted upon heat sink block (26) of the electro-luminescence panel (11) (Fig. 4C). However, the Fig. 2 (the prior art of Kawada's patent) discloses the driving circuit board (23) is mounted on the non-display substrate (11), wherein there is no heat sink block. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the driving circuit board is mounted on the non-display substrate without the heat sink block as taught by prior art Fig. 2, in the system of Kawada in order reduce the thickness for the display. Therefore, it is believed that the ground of the rejection is maintained.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer T. Nguyen whose telephone number is 571-272-7696. The examiner can normally be reached on Mon-Fri: 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick N. Edouard can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer Nguyen

06/19/05



REGINA LIANG
PRIMARY EXAMINER